Amendments to the Drawings:

Applicants have amended Figs. 1A-1D to label these drawings as "Prior Art". The replacement sheet containing revised Figs. 1A-1D is attached at the end of this paper.

REMARKS

Claims 1-3, 5-7, 9-11, 13-16 and 21-34 are pending. Claims 17-20 have been previously cancelled. Claims 4, 8, and 12 are cancelled by the present amendment. Claims 1-3, 5-7, 9-11 and 13-16 have been amended, and new claims 21-34 have been added. Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

Objection to the Drawings

Figs. 1A to 1D were objected to for lack of a prior art legend designated. Applicants have labeled "Prior Art" in these drawings, as shown in the Replacement Sheet.

The drawings were objected to for failing to show that a shoulder has a pair of shoulders. Applicants have amended paragraphs [0041], [0045] and [0055] of the specification to replace the wording "a shoulder 66b" with "at least one shoulder 66b" in order to reflect the feature that in one embodiment of the present invention a shoulder (see Fig. 4B, for example) is provided, while in another embodiment two shoulders (see Fig. 3B, for example).

Applicants have also amended paragraphs [0041] and [0042] to correct typographic errors.

Rejection under 35 U.S.C. § 112

Claims 4, 8 and 12 were rejected for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims have now been deleted in the currently amended claim.

Rejection under 35 U.S.C. § 102(e)

Claims 1, 2, 5, 6, 9, 10 and 13-16 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Kwon et al. (U.S. Publication 2004/0219715, hereinafter "Kwon"). Furthermore, Claims 1-3, 5-7, 9-11 and 13-15 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Kobayashi (U.S. Publication 2003/0183933, hereinafter

"Kobayashi").Applicants respectfully requests withdrawal of this rejection as it pertains to the amended set of claims and to the newly added claims.

1. Inventive features and advantages of the present invention

The present invention is directed to a microelectronic structure having a substrate of multiple conductive bumps for contact with bond pads on an electronic substrate. Each of the conductive bumps includes a conductive layer which is absent from at least one sidewall of the bump to prevent inadvertent short-circuiting between adjacent conductive bumps in the electronic assembly.

To achieve the above-mentioned advantage, the microelectronic structure in accordance with the present invention at least includes:

(1) a substrate;

(2) a plurality of conductive bumps formed on the substrate, each of the conductive bumps including an electrically insulative layer having an upper surface, a pair of sidewalls, an outer wall and an inner wall; and

(3) a conductive layer provided over the electrically insulative layer of each of the plurality of conductive bumps exposing at least one of the sidewalls.

Supporting descriptions for the inventive features can be seen, for example, in paragraphs [0037] to [0040].

2. Each of independent claims have been amended to recite the inventive features of the present invention

The above-mentioned inventive features are recited in the independent claims 1, 13, 21 and 27. Specifically, claim 1 has been amended to recite the features as follows.

a substrate comprising circuits;

a plurality of conductive bumps provided in adjacent relationship to each other on the substrate in electrical contact with the circuits, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface, a pair of sidewalls, an outer wall and an inner wall; and

a conductive layer provided over the electrically insulative layer of each of the plurality of conductive bumps,

wherein the conductive layer is absent from at least one of the sidewalls.(Emphasis added)

Claim 13 has been amended to recite the features as follows.

a substrate comprising circuits;

a plurality of conductive bumps provided in adjacent relationship to each other in rows on the substrate and in electrical contact with said circuits, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface, a pair of sidewalls, an outer wall and an inner wall;

a conductive layer provided over the electrically insulative layer of each of the plurality of conductive bumps, wherein the conductive layer is absent from at least one of the sidewalls; and

a protection layer provided on the substrate adjacent to the rows of the plurality of conductive bumps.(Emphasis added)

New Claim 21 recites the features as follows.

a substrate;

a plurality of conductive bumps formed on the substrate, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface and a side surface; and

a conductive layer formed over the electrically insulative layer of each of the plurality of conductive bumps exposing at least one portion of the side surface.(Emphasis added)

New Claim 27 recites the features as follows.

a first substrate;

a plurality of conductive pads formed on the first substrate;

a microelectronic structure including:

a second substrate;

a plurality of conductive bumps formed on the substrate corresponding to the plurality of conductive pads, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface and a side surface; and

a conductive layer formed over the electrically insulative layer of each of the plurality of conductive bumps exposing at least one portion of the side surface; and

a film disposed between the first substrate and the second substrate for electrically connecting the plurality of conductive bumps to the plurality of conductive pads.(Emphasis added)

3. Neither Kwon nor Kobayashi discloses or suggests the claimed invention

Kwon is directed to a bump 200 of a semiconductor chip 100 that comprises a bond pad 180, a conductive packing metal 220 formed on the bond pad 180, a conductive capping metal 230 formed on the conductive packing metal 220, and a sidewall insulating layer 210 formed on sidewalls of the conductive bump 200. Kwon therefore at least does not disclose or suggest a microelectronic structure that comprises an electrically insulative bump-forming layer formed of an electrically insulative having a side surface of which at least a portion is exposed by a conductive layer.

Kobayashi is directed to a semiconductor chip that comprises a bump electrode 100 formed over a main surface of the chip. The bump electrode 100, which is made of Au or Cu, etc., has at least one protrusion 101 on a top surface thereof. The protrusion 101 is higher than a peripheral portion 10b, where an inner lead is placed. Kobayashi therefore at least does not disclose or suggest a microelectronic structure that comprises an electrically insulative bump-forming layer formed of an electrically insulative having a side surface of which at least a portion is exposed by a conductive layer.

Accordingly, the rejections of independent claims 1 and 13 should be withdrawn. New independent claims 21 and 27 distinguish patentably over the cited references for the same reasons. All of the independent claims are therefore allowable.

4. Patentability of dependent claims

The dependent claims are believed to be patentable because they depend from allowable independent claims and because they recite additional patentable features.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the instant application, including claims 1-3, 5-7, 9-11, 13-16 and 21-34, is in condition for allowance. A Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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9/30/05
(Date)

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